WHAT IS CLAIMED IS:

1. An apparatus to detect errors in information stored in a processor resource, comprising:

an error detection component, the error detection component being configured to control the detection of errors in the information stored in the processor resource; and

a comparison component coupled to the error detection component, the comparison component being configured to receive the information from the processor resource, to determine if the information is valid, and to output a signal to indicate an error condition if the information is invalid.

2. The apparatus of claim 1, wherein the error detection component, comprises:

an error detection state machine (EDSM), the EDSM being configured to output a next-entry-to-read-out signal and a parity bit signal.

3. The apparatus of claim 2, wherein the EDSM, comprises:

a timer, the timer being configured to periodically output a next-entry-to-read-out signal to the processor resource;

a next pointer coupled to the timer, the next pointer being configured to contain a pointer value, which specifies a specific piece of information to be read out from the processor resource;

a move-to-processor-resource logic component coupled to the timer, the move-to-

processor-resource logic component being configured to prevent the next-entry-to-read-out signal from being sent by the timer if information is being moved into the processor resource;

a counter coupled to the move-to-processor-resource logic component, the counter is configured to count the number of shifts need to compute the proper parity bit; and

a parity and valid bits register coupled to the counter, the parity and valid bits register being configured to store at least one valid bit and parity bit pair.

4. The apparatus of claim 1, wherein the comparison component, comprises:

a shift register, the shift register being configured to receive the processor resource information and to output a parity bit for the processor resource information;

a first exclusive OR (XOR) gate coupled to the shift register, the first XOR gate being configured to receive the parity bit and a feedback signal and to output an indication of the validity of the parity bit; and

a second XOR gate coupled to the first XOR gate, the second XOR gate being configured to receive the parity bit signal and the indication of the validity of the parity bit and to output a machine check abort (MCA) if the parity bit signal and the indication of the validity of the parity bit indicate the processor resource information is invalid.

5. The apparatus of claim 4 further comprising

a result latch coupled between the first XOR gate and the second XOR gate, the result latch being configured to receive the indication of the validity of the parity bit from the first XOR gate, and to output a polarized signal, which indicates the validity of the parity bit.

6. The apparatus of claim 5, wherein the first XOR gate is configured to receive the polarized signal as the feedback signal.

7. The apparatus of claim 1, the result latch being further configured to transmit the polarized signal to the EDSM.

8. The apparatus of claim 1, wherein the processor resource is selected from at least the group comprising:

a cache;

at least one translation lookaside buffer (TLB);

at least one region identification (RID);

at least one protection key register;

at least one model specific register (MSR);

a control register access bus (CRAB) including at least one MSR coupled to the CRAB;

a CRAB coupled to at least one other CRAB;

a TLB coupled to a MSR which is coupled to a CRAB.

9. The apparatus of claim 8, wherein the CRAB further includes a checksum component coupled to the CRAB.

10. The apparatus of claim 8, wherein the CRAB including at least one MSR coupled to the CRAB further includes a checksum.

11. A method of protecting memory resources, comprising:

requesting information from a processor resource;

computing a parity bit value for the information;

comparing the computed parity bit value with an existing parity bit value associated with the information; and

if the computed parity bit value is not equal to the existing parity bit value, outputting a signal to indicate an error condition.

12. The method of claim 11, wherein requesting information from a processor resource comprises:

outputting a next-entry-to-read out signal.

13. The method of claim 12, wherein outputting a next-entry-to-read out signal comprises:

receiving a periodic read authorization signal;

determining if the processor resource is in use; and

outputting a next-pointer value indicating which item of information is to be read out, if the processor is not in use.

14. The method of claim 11, wherein computing a parity bit value for the read-out information, comprises:

receiving the requested information;

shifting-out the individual bits comprising the information;

computing a parity bit value for the read-out information; and

comparing the computed parity bit value with the existing parity bit value of the information.

15. The method of claim 11, wherein outputting a signal to indicate an error condition occurs if the computed parity bit value is different from the existing parity bit value.

16. The method of claim 11, wherein outputting a signal to indicate an error condition, comprises:

outputting a machine check abort (MCA) signal

17. An article of manufacture comprising a computer-readable medium having stored thereon instructions adapted to be executed by a processor, the instructions which, when executed, define a series of steps to protect processor resources, said steps comprising:

requesting information from a processor resource;

computing a parity bit value for the information;

comparing the computed parity bit value with an existing parity bit value associated with the information; and

if the computed parity bit value is not equal to the existing parity bit value, outputting a signal to replace the information.

18. The article of manufacture of claim 17, wherein requesting information from a processor resource comprises:

outputting a next-entry-to-read out signal.

19. The article of manufacture of claim 18, wherein outputting a next-entry-to-read out signal comprises:

receiving a periodic read authorization signal;

determining if the processor resource is in use; and

outputting a next-pointer value indicating which item of information is to be read out, if the processor is not in use.

20. The article of manufacture of claim 17, wherein computing a parity bit value for the read-out information, comprises:

receiving the requested information;

shifting-out the individual bits comprising the information;

computing a parity bit value for the read-out information; and

comparing the computed parity bit value with the existing parity bit value of the information.

21. The article of manufacture of claim 17, wherein outputting a signal to indicate an error condition occurs if the computed parity bit value is different than the existing parity bit value.

22. The article of manufacture of claim 17, wherein outputting a signal to indicate an error condition, comprises:

outputting a machine check abort (MCA) signal